FORM PTO-1390
(REV. 11-94)

U S DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

ATTORNEY'S DOCKET NUMBER
8479-039

09/509171

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB98/03373	November 11, 1998	November 13, 1997

TITLE OF INVENTION
Peripheral Servicing

APPLICANT(S) FOR DO/EO/US
Brian James Knight and Gert VanLoo

Applicant herewith submits to the United States Designated/ Elected Office (DO/EO/US) the following items under 35 U.S.C. 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the international Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureaus.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 37(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unexecuted).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☐ Other items or information:

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE
PCT/GB98/03373 09/509171	November 11, 1998

17. ☒ The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS				
(1)FOR	(2)NUMBER FILED	(3)NUMBER EXTRA	(4)RATE	(5)CALCULATIONS
TOTAL CLAIMS	20 - 20	0	X $ 18.00	$ 0.00
INDEPENDENT CLAIMS	1 - 3	0	X $ 78.00	0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $ 260.00	$ 0.00

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)): **CHECK ONE BOX ONLY** ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $ 670	
☐ No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... $ 760	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4) ..... $ 96	
☒ Filing where search report prepared by EPO or JPO ..... $ 840	$ 840.00
Surcharge of $130.00 for furnishing the National fee or oath or declaration later than 20 30 mos. from the earliest claimed priority date (37 CFR 1.492(e)).	
TOTAL OF ABOVE CALCULATIONS	= 840.00
Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (Note 37 CFR 1.9, 1.27, 1.28).	- $ 0.00
SUBTOTAL	= 840.00
Processing fee of $130.00 for furnishing the English Translation later than 20 30 mos. from the earliest claimed priority date (37 CFR 1.492(f)).	+
TOTAL FEES ENCLOSED	$ 840.00

a. ☐ A check in the amount of $__ to cover the above fees is enclosed.

b. ☒ Please charge Deposit Account No. 16-1150 in the amount of $840.00 to cover the above fees. A copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 16-1150. A copy of this sheet is enclosed.

18. ☐ Other instructions
n/a

19. ☒ All correspondence for this application should be mailed to
PENNIE & EDMONDS LLP
1155 AVENUE OF THE AMERICAS
NEW YORK, NEW YORK 10036-2711

20. ☒ All telephone inquiries should be made to (212) 790-9090

Rory J. Radding	U.S. Reg. No. 36,196 for Rory J. Radding	28,749	3/21/00
NAME	SIGNATURE	REGISTRATION NUMBER	DATE

Express Mail No.:EL 394 217 815 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Brian James Knight and Gert Van Loo

Application No.: TBA		Group Art Unit: TBA
Filed:	Herewith	Examiner: TBA
For:	PERIPHERAL SERVICING	Attorney Docket No.: 8479-039

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please enter the following preliminary amendment in the above-identified application.

AMENDMENT

IN THE CLAIMS

Please amend claims 1-8 as follows:

1. (amended) A computer system comprising:

a CPU; [which services]

a plurality of peripheral devices serviced by the CPU[,];

the CPU having a scheduling controller which includes [(a)] priority setting means and round robin register means;

the priority setting means being associated with each of the peripheral devices for setting a selected priority level [in device status register means], and including device status register means in which the priority level is set;

[and (b)] the round robin register means having marker means for selecting the next [device] one of the peripheral devices to be serviced by the CPU, and also having advancing means for advancing the marker in the round robin register means to [the] a next [device] one of the peripheral devices at [the] a highest priority level in [said] the device status register means;

[characterised in that said] the peripheral devices [each] having respective priority setting means [which set] for setting the priority level for [that device] the respective one of the peripheral devices, depending on the urgency with which that device requires servicing.

2. A computer system according to claim 1, wherein the device status register means includes a separate device status register [is provided] for each of the priority [level] levels, [in the respective device status register means, and a corresponding] and wherein the round robin register [is provided in the round robin register means for each device status register] means includes a plurality of round robin registers, a corresponding one of the round robin registers being provided for each of the device status registers;[,] each round robin register containing a single bit; the computer system further including priority determining means for identifying [the] a highest priority level device status register with at least one bit set; [and means in] the marker advancing means also including means for advancing the marker in the round robin register means at [the] a highest active priority level.

3. (amended) A computer system according to [either previous] claim 1, wherein different ones of the peripheral devices have different sets of priority levels.

4. (amended) A computer system according to claim 3, wherein the peripheral devices are communication devices containing buffers and [the] wherein priority level signals are determined by the state of occupancy of their buffers.

5. (amended) A computer system according to claim 4, wherein some of the peripheral devices which receive data at a higher rate[, or have a smaller buffer,] may switch to a higher priority level at lower levels of buffer occupancy [(or emptiness in the case of an output device)] than others.

6. (amended) A computer system according to claim [4 or] 5, wherein when [a device] one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower priority level.

7. (amended) A computer system according to [any preceding] claim 6, wherein lock-out of the devices is prevented by raising the device priority as servicing becomes more urgent, and once all devices at the highest active priority level are fully serviced, the priority level is dropped to a lower level, and servicing of devices at that level recommences; servicing of devices at the new lower level recommencing at a point where it was left off when a higher priority level up became active.

8. (amended) A computer system according to [any preceding] claim 6, wherein the system includes means for allocating more system resources to the CPU in response to detection that one or more devices are becoming in need of urgent servicing.

Please add the following claims.

9. (new) A computer system according to claim 2, wherein different ones of the peripheral devices have different sets of priority levels.

10. (new) A computer system according to claim 9, wherein the peripheral devices are communication devices containing buffers and wherein priority level signals are determined by the state of occupancy of their buffers.

11. (new) A computer system according to claim 10, wherein some of the peripheral devices which receive data at a higher rate may switch to a higher priority level at lower levels of buffer occupancy than others.

12. (new) A computer system according to claim 11, wherein when one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower priority level.

13. (new) A computer system according to claim 1, wherein the priority setting means is operable to raise priority of the respective peripheral device, as servicing becomes more urgent, for preventing lockout of the peripheral device; and wherein the priority setting means is operable to drop the priority level to a lower level once all of the peripheral devices at the highest active priority level are fully serviced, whereby servicing of the peripheral devices at that level recommences; servicing of the peripheral devices at a new lower level recommencing at a point where it was left off when a higher priority level became active.

14. (new) A computer system according to claim 1, further including means for allocating more system resources to the CPU in response to detection of a state wherein one or more of the peripheral devices are becoming in need of urgent servicing.

15. (new) A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower levels of buffer occupancy than others.

16. (new) A computer system according to claim 4, wherein some of the peripheral devices which transmit data at a higher rate may switch to a higher priority level at higher levels of buffer occupancy than others.

17. (new) A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for transmitting data may switch to a higher priority level at higher levels of buffer occupancy than others.

18. (new) A computer system according to claim 10, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower levels of buffer occupancy than others.

19. (new) A computer system according to claim 10, wherein some of the peripheral devices which transmit data at a higher rate may switch to a higher priority level at higher levels of buffer occupancy than others.

20. (new) A computer system according to claim 10, wherein some of the peripheral devices which have a smaller buffer for transmitting data may switch to a higher priority level at higher levels of buffer occupancy than others.

REMARKS

By this preliminary amendment, applicants respectfully request that the claims as filed be amended as described above. The claim amendments have been made to remove multiple dependencies from the claims and further clarify the claimed invention. None of the amendments have been made to overcome prior art.

Respectfully submitted,

H. C. Zelony Reg. No. 36,196

Date 3/21/00

for Rory J. Radding 28,749

Rory J. Radding (Reg. No.)

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Peripheral Servicing

The present invention relates to computer systems, and more particularly to scheduling of servicing of peripherals calling for attention in such systems.

In many computer systems, there is processing unit of some kind (which we will call a central processing unit, CPU) and a plurality of peripherals (which term may include any device outside the CPU core) which compete to be serviced by the CPU. A typical example is in a message switching system where there is a plurality of channels with messages arriving on some channels and being sent out on others. For each channel, there will be a buffer. Incoming data accumulates in the buffers of receiving channels, and has to be transferred from those buffers to a central memory; outgoing data is fed out to the outgoing channels from the buffers of those channels, and the outgoing data has to be passed to those buffers from the central memory.

The data flows between the buffers and the central memory are controlled by the CPU. These data flows (more specifically, the data flow rates for the various channels) are likely to be highly variable. Poor scheduling control by the CPU may result in the buffers of outgoing channels underflowing and, more seriously, in the buffers of incoming channels overflowing, which can lead to data loss.

Similar scheduling problems can arise more widely, in other types of computer system.

One technique for scheduling in such situations is to assign priorities to the various devices. The CPU effectively scans or polls the devices, starting with the highest priority device. As soon as the CPU finds a device requiring servicing, it services the device; it then resumes the polling of the devices from the beginning (ie from the highest priority device) again.

If the priority sequence is fixed, it is usually hard-wired (ie defined by hardware). If it is desired to make the priority sequence adjustable, then it can be implemented by software, eg using a table which defines the priority sequence of the various devices. However, that involves a certain amount of CPU overhead and delay, and is generally not preferred.

A drawback of such priority based techniques is that a low priority device may be starved of service indefinitely, if higher priority devices keep demanding servicing before the CPU's scanning can reach the low priority device.

An alternative technique has therefore been developed, in which the CPU polls cyclically through the devices. Each time the CPU encounters a device needing servicing, it services that device; it then resumes its polling of the devices from that device onwards. This technique is termed the round robin technique.

In the round robin technique, all devices effectively have equal priority. There is therefore no additional flexibility to be gained by implementing it by software. Since software implementation involves additional CPU overheads and delays, the round robin technique is therefore normally implemented by hardware, using a pair of registers and associated logic circuitry. There is a device status register, with one bit for each device (ie incoming or outgoing channel). When a device needs servicing, it sets this bit (and clears it when it no longer needs servicing). There is also a round robin register, with the same number of bits as the device status register.

A single bit is set in the round robin register, and determines which device the CPU services. Each time the CPU finishes servicing a device, the bit in the round robin register is advanced to the position of the next set bit in the device status register (both registers are effectively cyclic). If no devices call for servicing, the device status register will have no bits set; the round robin register is then normally maintained with its single bit in the position matching the last device to be serviced; as soon as another device requires servicing, the corresponding bit is

set in the device status register, and the bit in the round robin register is immediately advanced to the corresponding position.

The drawback of the round robin technique is precisely that all devices have effectively equal priorities. If a particular device has a high activity, then when the CPU has finished servicing it, it is desirable for it to be serviced again fairly soon. But with the round robin technique, all the other devices are effectively polled before the first device is reached again. If many of those other devices happen to require servicing, then they will all be serviced before the first device is reached again, even though their servicing could in fact be safely postponed, and the first device may by that time have overflowed.

EP-A-0339782 describes a system for achieving fixed priority, round robin or some combination of the two by means of a counter with programmable limits. The counter is incremented or decremented synchronously with the available time slots. US-A-5072363 is a variation on the latter technique in that it achieves different levels of service by using a counter to change the arbitration behaviour in a deterministic manner.

The general object of the present invention is to improve scheduling to alleviate or overcome the problems in the prior art. This is achieved by providing a computer system in which scheduling provides advantages of both the priority and round robin techniques and the devices can request servicing at different priority levels depending on their dynamic state, this state being internal to the device and not related to any central bus in the system. .

The invention is defined by the following claims.

A feature of the invention is that each peripheral device has associated with it (which may include a component integrated with the device) means arranged to produce a priority level signal which is indicative of the urgency with which that device needs servicing. For example, if three priority levels are used in a message

switching system, a receiving device may produce a priority level 3 signal (low priority) when its buffer is not empty, a priority level 2 signal (medium priority) when its buffer is half full, and a priority level 1 signal (high priority) when its buffer is nearly full. A transmitting device may produce a priority level 3 signal (low priority) when its buffer is nearly full, a priority level 2 signal (medium priority) when its buffer is half full, and a priority level 1 signal (high priority) when its buffer is nearly empty. Of course, these are just examples; fewer (2 priority levels) or more may be employed, and the conditions for signalling the various levels may vary from device to device. In particular, some devices which receive data at a higher rate, or have a smaller buffer may switch to a higher priority level at lower levels of buffer occupancy (or emptiness in the case of an output device) than others. There will be no signal when the buffer is completely empty for a receiving device, or completely full for a transmitting device.

It is preferred that a device should only produce a single priority level signal at a time. However, it is possible that when a device produces a signal of the appropriate priority level, it may produce signals of lower priority level as well (so for example a level 2 priority signal will be automatically accompanied by a level 3 priority signal). This will not have a significant effect on the way in which the present system operates.

It will of course be realized that not all devices may need to produce priority level signals of all levels. For instance, a transmitting device may not be able to produce a priority signal of as high a level as a receiving device, because the consequences of underflow in a transmitting device buffer will often be less serious than the consequences of overflow in a receiving device buffer.

The devices pass their priority level signals to a device status register means which stores these signals. Associated with this means there is a round robin register means. In a standard round robin register, there is a marker bit which is advanced, each time a device is serviced, from that device to the next device needing servicing. In the present round robin register means, the marker bit is

advanced from the current device to the next device at the highest active priority level.

The device status register means preferably consists of a separate device status register for each of the possible priority levels, and the round robin register means preferably consists of a corresponding or associated round robin register for each device status register, each containing the standard single bit.

When a device produces a priority signal, it sets the corresponding bit in the corresponding device status register. The device status registers are monitored to identify the highest priority level register with at least one bit set. The associated round robin register for that level is then used to determine which device the CPU should service next, and its bit is advanced to the next device (if any) at that priority level, ie to the next device in the corresponding device status register.

Thus in the present system, devices are normally processed in round robin fashion. However, the system also operates at a plurality of priority levels. Only devices at the highest active priority level are eligible for servicing.

However, no device is ever locked out indefinitely. Lock-out of devices is prevented in two ways. As the servicing of a device becomes more urgent, the device priority level is raised; and once all devices at the highest active priority level are fully serviced, the priority level drops to the next level down, and servicing of devices at that level recommences. It should be noted that in this latter situation, the servicing of devices at the new lower level recommences at the point where it was left off when the next priority level up became active. In other words, the position of the bit in each round robin register is frozen when the system enters a higher priority level. In fact, the devices will only enter the higher priority levels when the system is heavily loaded. As described in our concurrently filed application bearing reference PDC/20020, incorporated herein by reference, the system may include means for allocating more system resources to the processor in response to detection that one or more devices are becoming in need

of urgent servicing.

A computer system embodying the invention will now be described, by way of example, with reference to the drawings, in which:

Fig. 1 is a simplified block diagram of the system; and

Fig. 2 is a simplified block diagram of the scheduling means.

Referring to Fig. 1, the system comprises a set of devices 10-1 to 10-n, a CPU 11, and a memory 12. The devices 10 are communication devices, devices 10-1 and 10-2 being transmitting devices receiving data from the CPU and device 10-n being a receiving device feeding data to the CPU. It will be understood that the arrowheads on the couplings between the devices and the CPU show the direction of data flow; there are control signals flowing from all devices to the CPU and vice versa.

Each device includes a buffer BUFF, and priority setting means which monitors the occupancy of the buffer and generates a priority level signal accordingly. For a transmitting device such as devices 10-1 and 10-2 the priority setting means produces a priority level 3 signal (low priority) when its buffer is nearly full, a priority level 2 signal (medium priority) when its buffer is half full, and a priority level 1 signal (high priority) when its buffer is nearly empty. For receiving devices such as device 10-n the priority setting means produces a priority level 3 signal (low priority) when its buffer is not empty, a priority level 2 signal (medium priority) when its buffer is half full, and a priority level 1 signal (high priority) when its buffer is nearly full. There will be no signal when the buffer is completely empty for a receiving device, or completely full for a transmitting device.

The CPU 11 includes scheduling means 13 which receive the priority signals from the devices 10 and determine which device the CPU will service next.

The scheduling means are shown in more detail in Fig. 2.

There are 3 device status registers 20-1, 20-2, and 20-3, one for each of the 3 priority levels. Each device status register has the same number of positions (bits) as the number of devices 10, one position for each device. The device status registers are fed with the priority level signals from the devices, so that when a device produces a priority level signal, the corresponding position in the corresponding device status register is set (and cleared when the device clears its priority level signal). The 3 device status registers thus together store the priority levels of the devices.

There is also a round robin register means consisting of a set of round robin register 21-1 to 21-3, one for each of the device status registers. Each of the round robin registers contains a single bit, whose position corresponds to a set bit in the associated device status register. The position of this bit in a selected one of the round robin registers determines which device will next be serviced by the CPU. When a device is so serviced and its priority level signal is cleared, the bit in that round robin register is advanced to correspond to the next set bit in the corresponding device status register.

The selection of the round robin register in the round robin register means for this is performed as follows.

A priority determining circuit 22 is fed from all the device status registers 20, and determines what the highest active priority is. If there is any bit set in the highest priority device status register 20-1, the highest priority is 1; if there is no bit set in the highest priority device status register 20-1, but any bit is set in the middle priority device status register 20-2, the highest priority is 2; if there is no bit set in the highest priority device status register 20-1 or the middle priority device status register 20-2 but any bit is set in the low priority device status register 20-3, the highest priority is 3. (If none of the device status registers has any bit set, then there is no device requiring service from the CPU.)

The priority determining circuit 22 enables the corresponding round robin register 21. This allows the set bit in the enabled register to advance to the position corresponding to the next set bit in the corresponding device status register, as described above.

The priority determining circuit 22 also controls a gate circuit 23, which couples the appropriate one of the round robin circuits 21 to an overall round robin circuit 24. This overall round robin circuit therefore contains a single bit, whose position matches that of the bit in the round robin circuit with the highest active priority. This information is conveyed to the CPU 11 at the appropriate time, for example in response to a read of this register by the CPU, or following an interrupt scheduled to ensure regular servicing of peripherals, and the CPU thereupon services the device corresponding to this set bit.

Claims

1. A computer system comprising a CPU which services a plurality of peripheral devices, the CPU having a scheduling controller which includes (a) priority setting means associated with each of the devices for setting a selected priority level in device status register means; and (b) round robin register means having marker means for selecting the next device to be serviced by the CPU, and means for advancing the marker in the round robin register means to the next device at the highest priority level in said device status register means; characterised in that said peripheral devices each have respective priority setting means which set the priority level for that device depending on the urgency with which that device requires servicing.

2 A system according to claim 1, wherein a separate register is provided for each priority level in the respective device status register means, and a corresponding round robin register is provided in the round robin register means for each device status register, each round robin register containing a single bit; the system further including priority determining means for identifying the highest priority level device status register with at least one bit set; and means in the marker advancing means for advancing the marker in the round robin register means at the highest active priority level.

3. A system according to either previous claim, wherein different devices have different sets of priority levels.

4. A system according to Claim 3, wherein the devices are communication devices containing buffers and the priority level signals are determined by the state of occupancy of their buffers.

5. A system according to claim 4, wherein some devices which receive data at a higher rate, or have a smaller buffer may switch to a higher priority level at

lower levels of buffer occupancy (or emptiness in the case of an output device) than others.

6. A system according to claim 4 or 5, wherein when a device produces a signal of the appropriate priority level, it may produce signals of lower priority level.

7. A system according to any preceding claim, wherein lock-out of the devices is prevented by raising the device priority as servicing becomes more urgent, and once all devices at the highest active priority level are fully serviced, the priority level is dropped to a lower level, and servicing of devices at that level recommences; servicing of devices at the new lower level recommencing at a point where it was left off when a higher priority level up became active.

8. A system according to any preceding claim, wherein the system includes means for allocating more system resources to the CPU in response to detection that one or more devices are becoming in need of urgent servicing.

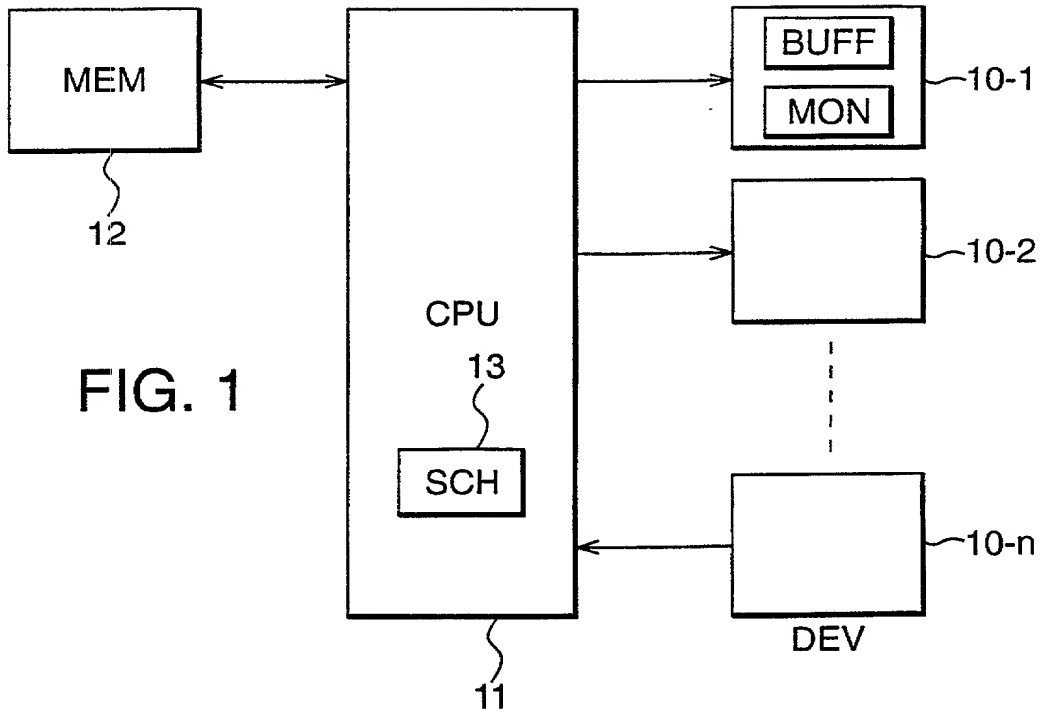
MEM
12
CPU
13
SCH
11
BUFF
MON
10-1
10-2
10-n
DEV

FIG. 1

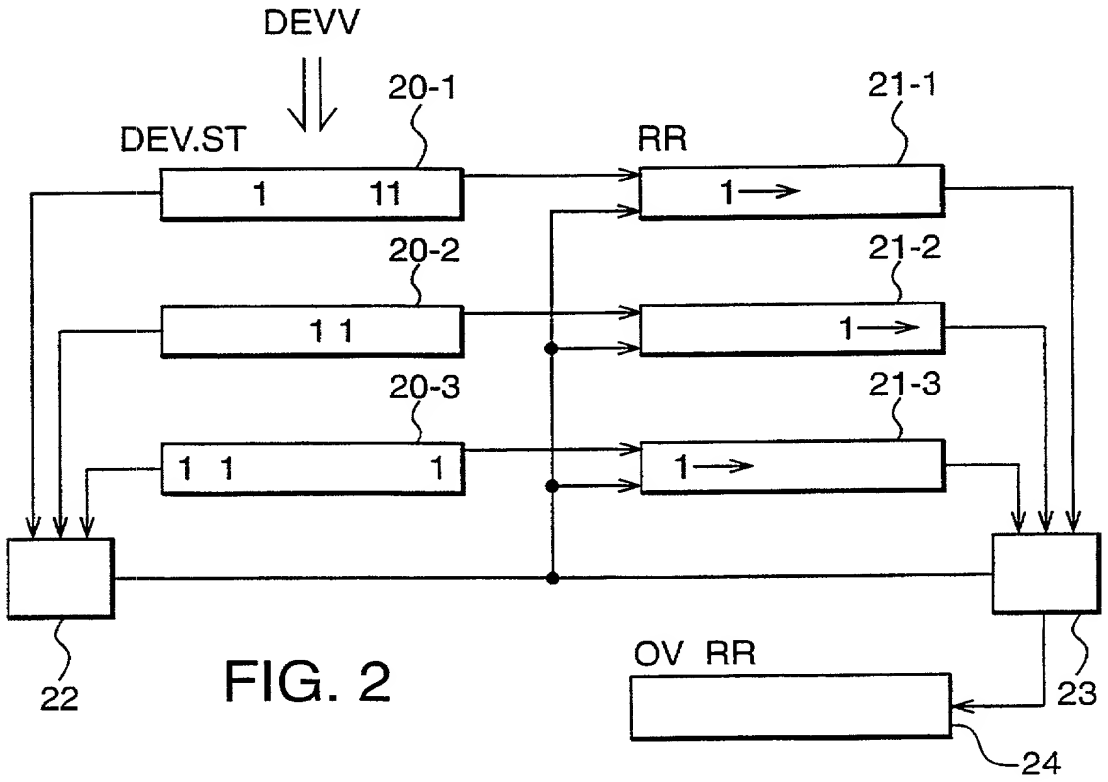
DEVV
DEV.ST
20-1
1 11
20-2
1 1
20-3
1 1 1
RR
21-1
1
21-2
1
21-3
1
22
23
OV RR
24

FIG. 2

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below at 201 et seq. underneath my name.

I believe I am the original, first and sole inventor if only one name is listed at 201 below, or an original, first and joint inventor if plural names are listed at 201 et seq. below, of the subject matter which is claimed and for which a patent is sought on the invention entitled

Peripheral Servicing

and for which a patent application:
☐ is attached hereto and includes amendment(s) filed on *(if applicable)*
☒ was filed in the United States on March 21, 2000 as Application No. 09/509,171, with a preliminary amendment filed the same day
☒ was filed as PCT international Application No. PCT/GB98/03373 on November 11, 1998 and was amended under PCT Article 19 on *(if applicable)*

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
9724030.3	United Kingdom	November 13, 1997	YES ☒ NO ☐
PCT/GB98/03373	PCT	November 11, 1998	YES ☒ NO ☐

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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